N-WAY PSEUDO CROSS-BAR USING DISCRETE PROCESSOR LOCAL BUSSES

ABSTRACT

A bus architecture is provided to facilitate communication between independent bus masters and independent bus slaves by having two or more bus arbiters in a system-on-chip (SOC) system. Each bus master in the system is coupled to all bus arbiters in the system, so that each bus master can access a corresponding bus slave concurrently as well as sequentially. Such concurrent communication carries not only read and/or write data but also a target address of the corresponding bus slave, thereby enabling true concurrency in data communication between bus masters and bus slaves.